1) Enter a single keyword, phrase, or Boolean expression.
Example: acoustic imaging (means the phrase acoustic imaging plus any stem variations)
2) Limit your search by using search operators and field codes, if desired.
Example: optical <and> (fiber <or> fibre) <in> ti
3) Limit the results by selecting Search Options.
4) Click Search. See Search Examples

"switch level simulator"

Start Search Clear

Note: This function returns plural and suffixed forms of the keyword(s).

Search operators: <and> <or> <not> <in> More

Field codes: au (author), ti (title), ab (abstract), jn (publication name), de (index term) More

Search Options:

Select publication types:
- [x] IEEE Journals
- [x] IEE Journals
- [x] IEEE Conference proceedings
- [x] IEE Conference proceedings
- [x] IEEE Standards

Select years to search:
From year: All to Present

Organize search results by:
Sort by: Year
In: Ascending order
List 50 Results per page

Your search matched **39** of **990765** documents.

A maximum of **39** results are displayed, **50** to a page, sorted by **publication year** in **ascending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **RELIANT: a reliability analysis tool for VLSI interconnects**
Frost, D.F.; Poole, K.F.; Haeussler, D.A.;
Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988 , 16-19 May 1988
Page(s): 27.8/1 -27.8/4

[Abstract] [PDF Full-Text (220 KB)] **IEEE CNF**

2 **A mixed-mode analog-digital simulation methodology for full custom designs**
Lee, E.S.; Fang, T.-F.;
Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988 , 16-19 May 1988
Page(s): 3.5/1 -3.5/4

[Abstract] [PDF Full-Text (360 KB)] **IEEE CNF**

3 **A unified mixed-mode digital/analog simulation environment**
Odryna, P.;
Circuits and Systems, 1988., IEEE International Symposium on , 7-9 June 1988
Page(s): 893 -896 vol.1

[Abstract] [PDF Full-Text (232 KB)] **IEEE CNF**

4 **For incremental circuit analysis using extracted hierarchy**
Beatty, D.L.; Bryant, R.E.;
Design Automation Conference, 1988. Proceedings., 25th ACM/IEEE , 12-15 June 1988
Page(s): 495 -500

[Abstract] [PDF Full-Text (500 KB)] **IEEE CNF**

---

5 **CHAMP: concurrent hierarchical and multilevel program for simulation of VLSI circuits**
Saab, D.G.; Mueller-Thuns, R.B.; Blaauw, D.; Abraham, J.A.; Rahmeh, J.T.;
Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers., IEEE International Conference on , 7-10 Nov. 1988
Page(s): 246 -249

[Abstract] [PDF Full-Text (316 KB)] **IEEE CNF**

---

6 **Data parallel switch-level simulation**
Bryant, R.E.;
Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers., IEEE International Conference on , 7-10 Nov. 1988
Page(s): 354 -357

[Abstract] [PDF Full-Text (352 KB)] **IEEE CNF**

---

7 **Incremental switch-level analysis**
Beatty, D.L.; Bryant, R.E.;
Design & Test of Computers, IEEE , Volume: 5 Issue: 6 , Dec. 1988
Page(s): 33 -42

[Abstract] [PDF Full-Text (772 KB)] **IEEE JNL**

---

8 **Switch-level simulation and the pass transistor EXOR gate**
Svensson, C.M.; Tjarnstrom, R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 7 Issue: 9 , Sept. 1988
Page(s): 994 -997

[Abstract] [PDF Full-Text (288 KB)] **IEEE JNL**

---

9 **SLS-a fast switch-level simulator [for MOS]**
Barzilai, Z.; Beece, D.K.; Huisman, L.M.; Iyengar, V.S.; Silberman, G.M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 7 Issue: 8 , Aug. 1988
Page(s): 838 -849

[Abstract] [PDF Full-Text (1124 KB)] **IEEE JNL**

---

10 **A bounded delay race model**
Seger, C.-J.;
Computer-Aided Design, 1989. ICCAD-89. Digest of Technical Papers., 1989 IEEE International Conference on , 5-9 Nov. 1989
Page(s): 130 -133

[Abstract] [PDF Full-Text (316 KB)] **IEEE CNF**

11 **Verifying pipelined hardware using symbolic logic simulation**
Bose, S.; Fisher, A.L.;
Computer Design: VLSI in Computers and Processors, 1989. ICCD '89. Proceedings., 1989 IEEE International Conference on , 2-4 Oct. 1989
Page(s): 217 -221

[Abstract] [PDF Full-Text (324 KB)] **IEEE CNF**

12 **CURRANT: a current prediction software tool using a switch-level simulator**
Haeussler, D.A.; Poole, K.F.;
Southeastcon '89. Proceedings. 'Energy and Information Technologies in the Southeast'., IEEE , 9-12 April 1989
Page(s): 946 -948 vol.3

[Abstract] [PDF Full-Text (208 KB)] **IEEE CNF**

13 **Performance analysis of CMOS ICs in total dose environments**
Kaul, N.; Bhuva, B.L.; Kerns, S.E.;
Southeastcon '89. Proceedings. 'Energy and Information Technologies in the Southeast'., IEEE , 9-12 April 1989
Page(s): 940 -945 vol.3

[Abstract] [PDF Full-Text (376 KB)] **IEEE CNF**

14 **KMIX: a mixed-mode simulator for analog/digital circuits using event driven waveform relaxation method**
Young-Hyun Jun; Song-Bai Park;
Circuits and Systems, 1989., IEEE International Symposium on , 8-11 May 1989
Page(s): 877 -880 vol.2

[Abstract] [PDF Full-Text (252 KB)] **IEEE CNF**

15 **A visually oriented architectural fault simulation environment for WSI**
Ryan, P.G.; Saab, D.G.; Kent Fuchs, W.;
Wafer Scale Integration, 1990. Proceedings., [2nd] International Conference on , 23-25 Jan. 1990
Page(s): 167 -173

[Abstract] [PDF Full-Text (296 KB)] **IEEE CNF**

16 **Detection of critical hazards in digital MOS VLSI circuits by switch-level timing simulation**
Sass, D.; Warmers, H.; Horneber, E.-H.;
Circuits and Systems, 1990., Proceedings of the 33rd Midwest Symposium on ,

12-14 Aug. 1990
Page(s): 584 -587 vol.1

[Abstract] [PDF Full-Text (228 KB)] **IEEE CNF**

---

17 **SNEL: a switch-level simulator using multiple levels of functional abstraction**
Blaauw, D.T.; Mueller-Thuns, R.B.; Saab, D.G.; Banerjee, P.; Abraham, J.A.;
Computer-Aided Design, 1990. ICCAD-90. Digest of Technical Papers., 1990 IEEE International Conference on , 11-15 Nov. 1990
Page(s): 66 -69

[Abstract] [PDF Full-Text (428 KB)] **IEEE CNF**

---

18 **Design of a scalable parallel switch-level simulator for VLSI**
Mueller-Thuns, R.B.; Saab, D.G.; Abraham, J.A.;
Supercomputing '90. Proceedings of , 12-16 Nov. 1990
Page(s): 615 -624

[Abstract] [PDF Full-Text (624 KB)] **IEEE CNF**

---

19 **Automatic modeling of switch-level networks using partial orders [MOS circuits]**
Agrawal, P.; Robinson, S.H.; Szymanski, T.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 9 Issue: 7 , July 1990
Page(s): 696 -707

[Abstract] [PDF Full-Text (1164 KB)] **IEEE JNL**

---

20 **Hybrid compiled/interpreted simulation of MOS circuits**
McMurchie, L.; Anderson, C.; Borriello, G.;
Design Automation. EDAC. Proceedings of the European Conference on , 25-28 Feb. 1991
Page(s): 558 -564

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

---

21 **On probabilistic switch-level simulation for asynchronous circuits**
Rajgopal, S.; Dyagi, A.;
Design Automation. EDAC. Proceedings of the European Conference on , 25-28 Feb. 1991
Page(s): 339 -343

[Abstract] [PDF Full-Text (432 KB)] **IEEE CNF**

---

22 **Massively parallel switch-level simulation: a feasibility study**
Kravitz, S.A.; Bryant, R.E.; Rutenbar, R.A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 10 Issue: 7 , July 1991
Page(s): 871 -894

[Abstract] [PDF Full-Text (2368 KB)] **IEEE JNL**

---

23 **Formal verification of memory circuits by switch-level simulation**
Bryant, R.E.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 10 Issue: 1 , Jan. 1991
Page(s): 94 -102

[Abstract] [PDF Full-Text (832 KB)] **IEEE JNL**

---

24 **New switch level simulator: analysis of a general switched network to avoid limit cycle for switching control**
Mizutani, H.; Tanaka, M.;
Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on , 9-12 Aug. 1992
Page(s): 560 -563 vol.1

[Abstract] [PDF Full-Text (168 KB)] **IEEE CNF**

---

25 **Distributed VLSI simulation on a network of workstations**
Karthik, S.; Abraham, J.A.;
Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceedings., IEEE 1992 International Conference on , 11-14 Oct. 1992
Page(s): 508 -511

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

---

26 **Power estimation tool for sub-micron CMOS VLSI circuits**
Rouatbi, F.; Haroun, B.; Al-Khalili, A.J.;
Computer-Aided Design, 1992. ICCAD-92. Digest of Technical Papers., 1992 IEEE/ACM International Conference on , 8-12 Nov. 1992
Page(s): 204 -209

[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

---

27 **Zero delay versus positive delay in an incremental switch-level simulator**
Jones, L.G.;
Design Automation Conference, 1992. Proceedings., 29th ACM/IEEE , 8-12 June 1992
Page(s): 424 -427

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

28 **Exploiting hierarchy in a cache-based switch-level simulator**
Jones, L.G.;
Design Automation, 1992. Proceedings. [3rd] European Conference on , 16-19 March 1992
Page(s): 207 -211

[Abstract] [PDF Full-Text (372 KB)] **IEEE CNF**

29 **A parallel switch-level simulator for mixed analog-digital circuit simulation**
Molin, B.-A.; Mattisson, S.;
Design Automation, 1992. Proceedings. [3rd] European Conference on , 16-19 March 1992
Page(s): 202 -206

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

30 **Piecewise linear models for Rsim**
Kao, R.; Horowitz, M.;
Computer-Aided Design, 1993. ICCAD-93. Digest of Technical Papers., 1993 IEEE/ACM International Conference on , 7-11 Nov. 1993
Page(s): 753 -758

[Abstract] [PDF Full-Text (512 KB)] **IEEE CNF**

31 **Reducing the scheduling cost in event-driven simulation through component clustering**
Blaauw, D.T.; Jones, L.G.;
Design Automation, 1993, with the European Event in ASIC Design. Proceedings. [4th] European Conference on , 22-25 Feb. 1993
Page(s): 18 -22

[Abstract] [PDF Full-Text (448 KB)] **IEEE CNF**

32 **Statistical degradation analysis of digital CMOS IC's**
Rangavajjhala, V.S.; Bhuva, B.L.; Kerns, S.E.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 12 Issue: 6 , June 1993
Page(s): 837 -844

[Abstract] [PDF Full-Text (684 KB)] **IEEE JNL**

33 **Timing analysis for piecewise linear Rsim**
Kao, R.; Horowitz, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 13 Issue: 12 , Dec. 1994

Page(s): 1498 -1512

[Abstract] [PDF Full-Text (1220 KB)] **IEEE JNL**

---

34 **Network initialization in a switch-level simulator**
van Genderen, A.J.;
European Design and Test Conference, 1995. ED&TC 1995, Proceedings. , 6-9 March 1995
Page(s): 596

[Abstract] [PDF Full-Text (64 KB)] **IEEE CNF**

---

35 **Set-and-see switch-level simulation for VLSI functional verification**
Smith, J.W.;
Circuits and Systems, 1996., IEEE 39th Midwest symposium on , Volume: 1 , 18-21 Aug. 1996
Page(s): 402 -405 vol.1

[Abstract] [PDF Full-Text (512 KB)] **IEEE CNF**

---

36 **A multidimensional study on the feasibility of parallel switch-level circuit simulation**
Yu-An Chen; Jha, V.; Bagrodia, R.;
Parallel and Distributed Simulation, 1997. Proceedings. 11th Workshop on , 10-13 June 1997
Page(s): 46 -54

[Abstract] [PDF Full-Text (912 KB)] **IEEE CNF**

---

37 **Algorithms for switch level delay fault simulation**
Bose, S.; Agrawal, V.D.; Szymanski, T.G.;
Test Conference, 1997. Proceedings., International , 1-6 Nov. 1997
Page(s): 982 -991

[Abstract] [PDF Full-Text (948 KB)] **IEEE CNF**

---

38 **Shared memory implementation of a parallel switch-level circuit simulator**
Chen, Y.-A.; Bagrodia, R.;
Parallel and Distributed Simulation, 1998. PADS 98. Proceedings. Twelfth Workshop on , 26-29 May 1998
Page(s): 134 -141

[Abstract] [PDF Full-Text (208 KB)] **IEEE CNF**

---

39 **Logic verification of very large circuits using Shark**
Casas, J.; Yang, H.; Khaira, M.; Joshi, M.; Tetzlaff, T.; Otto, S.; Seligman, E.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On , 7-10 Jan.

1999
Page(s): 310 -317

[Abstract] [PDF Full-Text (96 KB)] **IEEE CNF**

EAST SEARCH

3/11/04

L#	Hits	Search String	Databases
L1	378	(tri-state or tristate) and (hdl or vhdl)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	238	1 and (re-set$5 or reset$5)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	81	2 and inverter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	75	inverter and (hdl or vhdl) and unknown and initial$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Results of search set L3:

US 6704889 B2	Enhanced embedded logic analyzer	20040309	714/39
US 6701491 B1	Input/output probing apparatus and input/output probing method using the same, and mixed emulation/simulation method based on it	20040302	716/4
US 6694464 B1	Method and apparatus for dynamically testing electrical interconnect	20040217	714/725
US 6621298 B2	Variable grain architecture for FPGA integrated circuits	20030916	326/50
US 6598209 B1	RTL power analysis using gate-level cell power models	20030722	716/4
US 6574787 B1	Method and apparatus for logic synthesis (word oriented netlist)	20030603	716/18
US 6526558 B2	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	20030225	716/16
US 6526511 B1	Apparatus and method for modifying microprocessor system at random and maintaining equivalent functionality in spite of modification, and the same microprocessor system	20030225	713/190
US 6519755 B1	Method and apparatus for logic synthesis with elaboration	20030211	716/18
US 6493648 B1	Method and apparatus for logic synthesis (inferring complex components)	20021210	702/119
US 6470475 B2	Synthesizable synchronous static RAM	20021022	716/1
US 6460148 B2	Enhanced embedded logic analyzer	20021001	714/39
US 6421818 B1	Efficient top-down characterization method	20020716	716/18
US 6380759 B1	Variable grain architecture for FPGA integrated circuits	20020430	326/41
US 6378123 B1	Method of handling macro components in circuit design synthesis	20020423	716/18
US 6377912 B1	Emulation system with time-multiplexed interconnect	20020423	703/28
US 6348813 B1	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	20020219	326/41
US 6339539 B1	Content addressable memory having read/write capabilities that do not interrupt continuous search cycles	20020115	365/49

US 6295636 B1	RTL analysis for improved logic synthesis	20010925	716/18
US 6292931 B1	RTL analysis tool	20010918	716/18
US 6292764 B1	Tunable architecture for device adapter	20010918	703/14
US 6289498 B1	VDHL/Verilog expertise and gate synthesis automation system	20010911	716/18
US 6289491 B1	Netlist analysis tool by degree of conformity	20010911	716/5
US 6286114 B1	Enhanced embedded logic analyzer	20010904	714/39
US 6263483 B1	Method of accessing the generic netlist created by synopsys design compilier	20010717	716/18
US 6247147 B1	Enhanced embedded logic analyzer	20010612	714/39
US 6216257 B1	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	20010410	716/16
US 6211695 B1	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	20010403	326/40
US 6205572 B1	Buffering tree analysis in mapped design	20010320	716/5
US 6204686 B1	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	20010320	326/39
US 6184713 B1	Scalable architecture for high density CPLDS having two-level hierarchy of routing resources	20010206	326/41
US 6181163 B1	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control signals	20010130	326/41
US 6173435 B1	Internal clock handling in synthesis script	20010109	716/18
US 6150842 A	Variable grain architecture for FPGA integrated circuits	20001121	326/41
US 6130551 A	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	20001010	326/39
US 6127843 A	Dual port SRAM memory for run time use in FPGA integrated circuits	20001003	326/40
US 6107823 A	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	20000822	326/41
US 6097212 A	Variable grain architecture for FPGA integrated circuits	20000801	326/41
US 6081473 A	FPGA integrated circuit having embedded sram memory blocks each with statically and dynamically controllable read mode	20000627	365/230.01
US 6034544 A	Programmable input/output block (IOB) in FPGA integrated circuits	20000307	326/39
US 5990702 A	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VGBs) in FPGA integrated circuits	19991123	326/41
US 5982193 A	Input/output block (IOB) connections to MaxL lines, nor lines and dendrites in FPGA integrated circuits	19991109	326/39
US 5960191 A	Emulation system with time-multiplexed interconnect	19990928	703/28
US 5943490 A	Distributed logic analyzer for use in a hardware logic emulation system	19990824	703/28

US 5935256 A	Parallel processing integrated circuit tester	19990810	713/400
US 5931953 A	Parallel processing integrated circuit tester	19990803	713/500
US 5931952 A	Parallel processing integrated circuit tester	19990803	713/400
US 5923676 A	Bist architecture for measurement of integrated circuit delays	19990713	714/733
US 5920712 A	Emulation system having multiple emulator clock cycles per emulated clock cycle	19990706	703/23
US 5857109 A	Programmable logic device for real time video processing	19990105	712/37
US 5841663 A	Apparatus and method for synthesizing integrated circuits using parameterized HDL modules	19981124	716/18
US 5822564 A	Checkpointing in an emulation system	19981013	703/28
US 5812858 A	Method and apparatus for providing register and interrupt compatibility between non-identical integrated circuits	19980922	710/260
US 5751592 A	Apparatus and method of supporting functional design of logic circuit and apparatus and method of verifying functional design of logic circuit	19980512	716/5
US 5748642 A	Parallel processing integrated circuit tester	19980505	714/724
US 5696772 A	Test vector compression/decompression system for parallel processing integrated circuit tester	19971209	714/32
US 5644498 A	Timing shell generation through netlist reduction	19970701	716/2
US 5603043 A	System for compiling algorithmic language source code for implementation in programmable hardware	19970211	712/1
US 5581738 A	Method and apparatus for back-annotating timing constraints into simulation models of field programmable gate arrays	19961203	716/16
US 5577213 A	Multi-device adapter card for computer	19961119	710/100
US 5535342 A	Pld connector for module having configuration of either first PLD or second PLD and reconfigurable bus for communication of two different bus protocols	19960709	710/315
US 5499192 A	Method for generating logic modules from a high level block diagram	19960312	716/17
US 5497498 A	Video processing module using a second programmable logic device which reconfigures a first programmable logic device for data transformation	19960305	710/104
US 5425036 A	Method and apparatus for debugging reconfigurable emulation systems	19950613	714/735
US 5408235 A	Second order Sigma-Delta based analog to digital converter having superior analog components and having a programmable comb filter coupled to the digital signal processor	19950418	341/143
US 20030225955 A1	Data modem	20031204	710/306
US 20030208733 A1	RTL power analysis using gate-level cell power models	20031106	716/4
US 20030204822 A1	Digital logic optimization using selection operators	20031030	716/2
US 20030200510 A1	Digital circuits using universal logic gates	20031023	716/1
US 20030177457 A1	Optimization of digital designs	20030918	716/3
US 20030149953 A1	Integrated circuit cell library	20030807	716/17
US 20030126579 A1	Digital design using selection operations	20030703	716/18
US 20030074178 A1	Emulation system with time-multiplexed interconnect	20030417	703/25

US 20030023941 A1	Computer-aided design system to automate scan synthesis at register-transfer level	20030130	716/4
US 20020194543 A1	Enhanced embedded logic analyzer	20021219	714/39
US 20020186044 A1	Variable grain architecture for FPGA integrated circuits	20021212	326/41
US 20020177990 A1	Distributed logic analyzer for use in a hardware logic emulation system	20021128	703/28
US 20020161568 A1	Memory circuit for use in hardware emulation system	20021031	703/25
US 20020110042 A1	Synthesizable synchronous static RAM	20020815	365/233
US 20010056570 A1	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	20011227	716/16
US 20010037477 A1	Enhanced embedded logic analyzer	20011101	714/41

Results of search set L4:

US 6704889 B2	Enhanced embedded logic analyzer	20040309	714/39
US 6602469 B1	Health monitoring and diagnostic device and network-based health assessment and medical records maintenance system	20030805	422/68.1
US 6591402 B1	System and method for performing assertion-based analysis of circuit designs	20030708	716/5
US 6560757 B1	Method of verification	20030506	716/5
US 6557145 B2	Method for design optimization using logical and physical information	20030429	716/2
US 6543036 B1	Non-linear, gain-based modeling of circuit delay for an electronic design automation system	20030401	716/6
US 6526511 B1	Apparatus and method for modifying microprocessor system at random and maintaining equivalent functionality in spite of modification, and the same microprocessor system	20030225	713/190
US 6499129 B1	Method of estimating performance of integrated circuit designs	20021224	716/4
US 6467068 B1	Construction of a technology library for use in an electronic design automation system that converts the technology library into non-linear, gain-based models for estimating circuit delay	20021015	716/6
US 6460148 B2	Enhanced embedded logic analyzer	20021001	714/39
US 6446240 B1	Evaluation of a technology library for use in an electronic design automation system that converts the technology library into non-linear, gain-based models for estimating circuit delay	20020903	716/2
US 6421818 B1	Efficient top-down characterization method	20020716	716/18
US 6405348 B1	Deep sub-micron static timing analysis in the presence of crosstalk	20020611	716/4
US 6378123 B1	Method of handling macro components in circuit design synthesis	20020423	716/18
US 6341361 B1	Graphical user interface for testability operation	20020122	714/726
US 6295636 B1	RTL analysis for improved logic synthesis	20010925	716/18

US 6292931 B1	RTL analysis tool	20010918	716/18
US 6289498 B1	VDHL/Verilog expertise and gate synthesis automation system	20010911	716/18
US 6289491 B1	Netlist analysis tool by degree of conformity	20010911	716/5
US 6286114 B1	Enhanced embedded logic analyzer	20010904	714/39
US 6263483 B1	Method of accessing the generic netlist created by synopsys design compilier	20010717	716/18
US 6247165 B1	System and process of extracting gate-level descriptions from simulation tables for formal verification	20010612	716/5
US 6247147 B1	Enhanced embedded logic analyzer	20010612	714/39
US 6243848 B1	Process for analyzing complex structures and system for implementing a process of this type	20010605	716/1
US 6216252 B1	Method and system for creating, validating, and scaling structural description of electronic device	20010410	716/1
US 6205572 B1	Buffering tree analysis in mapped design	20010320	716/5
US 6173435 B1	Internal clock handling in synthesis script	20010109	716/18
US 6167561 A	Method and apparatus for entry of timing constraints	20001226	716/18
US 6141631 A	Pulse rejection circuit model program and technique in VHDL	20001031	703/14
US 6092233 A	Pipelined Berlekamp-Massey error locator polynomial generating apparatus and method	20000718	714/784
US 6086629 A	Method for design implementation of routing in an FPGA using placement directives such as local outputs and virtual buffers	20000711	716/12
US 5953235 A	Method for processing a hardware independent user description to generate logic circuit elements including flip-flops, latches, and three-state buffers and combinations thereof	19990914	716/18
US 5937190 A	Architecture and methods for a hardware description language source level analysis and debugging system	19990810	717/131
US 5923676 A	Bist architecture for measurement of integrated circuit delays	19990713	714/733
US 5910898 A	Circuit design methods and tools	19990608	716/1
US 5886929 A	High speed addressing buffer and methods for implementing same	19990323	365/189.05
US 5841674 A	Circuit design methods and tools	19981124	716/12
US 5748488 A	Method for generating a logic circuit from a hardware independent user description using assignment conditions	19980505	716/18
US 5737574 A	Method for generating a logic circuit from a hardware independent user description using mux conditions and hardware selectors	19980407	711/162
US 5691911 A	Method for pre-processing a hardware independent description of a logic circuit	19971125	716/18
US 5684808 A	System and method for satisfying mutually exclusive gating requirements in automatic test pattern generation systems	19971104	714/726
US 5680318 A	Synthesizer for generating a logic network using a hardware independent description	19971021	716/18

US 5661661 A	Method for processing a hardware independent user description to generate logic circuit elements including flip-flops, latches, and three-state buffers and combinations thereof	19970826	716/18
US 5598344 A	Method and system for creating, validating, and scaling structural description of electronic device	19970128	716/18
US 5581781 A	Synthesizer for generating a logic network using a hardware independent description	19961203	716/18
US 5537065 A	Programmable voltage detection system	19960716	327/50
US 5533123 A	Programmable distributed personal security	19960702	713/189
US 5499191 A	Multi-level logic optimization in programmable logic devices	19960312	716/17
US 4769753 A	Compensated exponential voltage multiplier for electroluminescent displays	19880906	363/60
US 4493076 A	Security system for a distributed control exchange	19850108	714/11
US 4242730 A	Single scan microprocessor-controlled densitometer	19801230	356/39
US 20030225955 A1	Data modem	20031204	710/306
US 20030212979 A1	Depopulated programmable logic array	20031113	716/16
US 20030154433 A1	Method and apparatus for broadcasting scan patterns in a scan-based integrated circuit	20030814	714/726
US 20030141936 A1	All-digital frequency synthesis with non-linear differential term for handling frequency perturbations	20030731	331/16
US 20030133522 A1	All-digital frequency synthesis with DCO gain calculation	20030717	375/345
US 20030107442 A1	All-digital frequency synthesis with capacitive re-introduction of dithered tuning information	20030612	331/1A
US 20030079190 A1	Method for deriving a hierarchical functional description of a circuit	20030424	716/4
US 20030035502 A1	Data reception circuit	20030220	375/372
US 20030016822 A1	Recursive cryptoaccelerator and recursive VHDL design of logic circuits	20030123	380/46
US 20020194543 A1	Enhanced embedded logic analyzer	20021219	714/39
US 20020189635 A1	Ultrasonic cleaning	20021219	134/1
US 20020189633 A1	Cleaning process which uses ultrasonic waves	20021219	134/1
US 20020188914 A1	Method for deriving a hierarchical functional description of a circuit	20021212	716/3
US 20020179124 A1	Ultrasonic implement	20021205	134/34
US 20020178285 A1	Method and apparatus for modeling dataflow systems and realization to hardware	20021128	709/237
US 20020144211 A1	Method and program product for detecting bus conflict and floating bus conditions in circuit designs	20021003	714/811
US 20020135408 A1	Method and interface for glitch-free clock switching	20020926	327/145
US 20020133325 A1	Discrete event simulator	20020919	703/17
US 20020120891 A1	Method for diagnosing failures using invariant analysis	20020829	714/724
US 20020059555 A1	Depopulated programmable logic array	20020516	716/16
US 20020022950 A1	Method and system for identifying inaccurate models	20020221	703/14
US 20020010903 A1	Programmable logic array embedded in mask-programmed ASIC	20020124	716/18

US 20010037477 A1	Enhanced embedded logic analyzer	20011101	714/41
US 20010010090 A1	Method for design optimization using logical and physical information	20010726	716/2